REMARKS/ARGUMENT

The applicant's attorneys appreciate the Examiner's thorough search and remarks.

The specification has been amended to make it consistent with the Figures.

Claims 9 was rejected under 35 U.S.C. §102(e) over Kinzer, U.S. Patent No. 5,731,604. Claim 9 provides for "etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said oxide". Spacing the stripes in a MOS semiconductor device manufactured according to the method of claim 9 provides for an unexpectedly improved figure of merit over the prior known devices.

Figure of merit is an important performance indicator in a MOS semiconductor device. The figure of merit is in part the product of R_{DSON} and Q_g of the device. As disclosed in the specification, in a MOS semiconductor device having a stripe topology, the Q_g is increased far less rapidly than in a MOS semiconductor device with a cellular topology as the spacing between the stripes is decreased. (See Fig. 10 and note the relatively shallower slope for a stripe topology.) However, the decrease in R_{DSON} is relatively more rapid in a MOS semiconductor device having a stripe topology than in a MOS semiconductor device having a cellular topology when the spacing between the stripes is changed between 1-4 microns. (See Fig. 9, and note the relatively more rapid rate of change of $1/R_{DSON}$ when the spacing is between about 1-4 microns). The comparison of R_{DSON} and Q_g in a MOS semiconductor device having a stripe topology to those of a MOS semiconductor device having a cellular topology indicates that proportionally the change in R_{DSON} in a MOS semiconductor device having a stripe topology is more rapid than the corresponding change in the Q_g of the device as the spacing between the stripes is changed between 1-4 microns. Also, despite a relatively rapid change in the R_{DSON} of a MOS semiconductor device having a stripe topology, the changes in Q_g are smaller as the spacing between the stripes changes from 1-4 microns as compared to a MOS semiconductor device having a cellular topology. Thus, as has been described in the specification, compared to a MOS semiconductor device having a cellular topology, a lower figure of merit results in a MOS semiconductor device of a stripe topology having stripes that are spaced 1-4 microns, which is the geometry produced by the method of claim 9. Neither Kinzer nor any other art of record, singly or in combination with another, shows or suggests the combination claimed in claim 9. Reconsideration of claim 9 is requested.

Claims 10-17 depend from claim 9, and, therefore, include at least its limitations. These claims include other limitations which in combination with those of claim 9 are not shown or suggested by the art of record.

For example, claim 16 provides for etching the polysilicon layer and the oxide layer to form polysilicon stripes that are spaced 1.5 microns apart. As explained in the specification a device produced by a method according to claim 9 reaches its practical minimum figure of merit when the stripes are spaced 1.5 microns apart. Spec. at 4, lines 1-2. This critical limitation is not shown or suggested by Kinzer or any other art of record.

As another example, claim 17 provides for etching the polysilicon and the oxide layer to form stripes that are spaced 1-4 microns apart and are 3.2-3.4 microns wide. As the specification states a choice of these dimensions results in a minimum figure of merit. Spec. at 10, lines 16-18. These critical limitations are not shown or suggested by Kinzer or any other art of record.

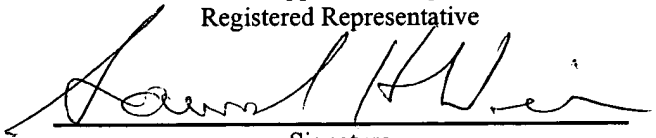
Reconsideration of claims 10-17 is requested.

The application is believed to be in condition for allowance. Such action is earnestly requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on November 7, 2001

Samuel H. Weiner

Name of applicant, assignee or Registered Representative



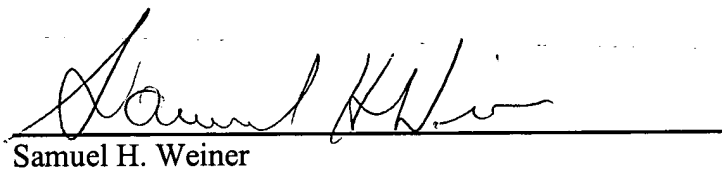
Signature

November 7, 2001

Date of Signature

SHW/KS:gl

Respectfully submitted,



Samuel H. Weiner
Registration No.: 18,510
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE

37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph at page 10, line 12 to page 10, line 15:

It has been found that the stripe geometry will produce a larger channel width per unit area for polyline spacings in the region between about 1 to 4 microns, particularly at about 1.5 microns, surprisingly with [no increase of R_{DSON}] a relatively small increase in Q_g.

CLAIMS:

9. (Twice Amended) The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said oxide; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; diffusing second base diffusion stripes, into said silicon surface, using said stripes of polysilicon as a mask, to a depth below that of said source diffusions and a width substantially equal to the space between the opposite edges of adjacent pairs of said polysilicon stripes.